AMENDMENTS TO CLAIMS

11. (Currently Amended) A method for sharing data between a first controller memory module and a second controller memory module, comprising:

providing a first shared path in a first channel interface module (CIM), wherein the shared path ~~has~~ includes a switchable component for determining which data is to be routed over the shared path;

wherein the first shared path is included on a data path between the first and second controller memory modules;

a direct memory access engine for each of said first and second controller memory modules; and

transferring first data between said first controller memory module and said second controller memory module using said direct memory access engine for at least one of the first and second controller memory modules, wherein said switchable component provides passage of said first data over said first shared path between the first and second controller memory modules.

12. (Currently Amended) The method of Claim 11, further comprising:

providing a second shared path in a second channel interface module;

wherein the second shared path is included on a data path between the first and second controller memory modules, and the second shared path includes a second switchable component for determining which data is to be routed over the second shared path; and

transferring second data between said first controller memory module and said second controller memory module using ~~each of~~ said direct memory access engine[[s]] in the first controller memory module and another direct memory access engine in the second controller memory module, wherein the second data passes through said second shared path.

13. (Currently Amended) The method of Claim 11, further comprising:

connecting said first ~~and second~~ channel interface module[[s]] ~~and~~ to both said first and second controller memory modules ~~to~~ via a passive backplane, wherein the first data passes through the passive backplane during said step of transferring.

14. (Currently Amended) An apparatus for sharing data between a first controller memory module and a second controller memory module, wherein each of the first and second controller memory modules is for controlling communication of storage data between one or more host computers and one or more storage devices, comprising:

at least a first channel interface module having a first shared path, wherein the shared path has a switchable component, operably associated therewith, for selecting which data is to be routed on the shared path;

a first controller memory module including a first direct memory access engine;

a second controller memory module including a second direct memory access engine; ~~and~~

wherein the first channel interface module is directed by at least one of the first and second controller memory modules to communicate with a first of the host computers and a first of the data storage devices, so that the first channel interface module is operational for sending and receiving storage data between the first host computer and the first storage device;

a communications interface to permit direct communications between said first and second controller memory modules; wherein data is transferred between said first and second controller memory modules using at least one of said first and second direct memory access engines, and using the switchable component ~~of said first shared path,~~ and wherein the direct communications are not routed through the first host computer.

15. (Previously Presented) The apparatus of Claim 14, further including:

a second channel interface module having a second shared path, wherein the second shared path has a second switchable component, operably associated therewith, for determining which data is to be routed over the second shared path;

wherein said second switchable component provides passage of second data over said second shared path between the first and second controller memory modules using each of said first and second direct memory access engines.

16. (Previously Presented) The apparatus of Claim 14, wherein:

said communications interface includes a passive backplane.

17. (Previously Presented) The apparatus of Claim 16, wherein:

said passive backplane includes at least first and second peripheral component interconnect (PCIX) buses.

18. (Previously Presented) The method of Claim 11, wherein the first shared path transmits the first data between the direct memory access engines of the first and second controller memory modules.

19. (Previously Presented) The method of Claim 11, further including providing a plurality of data buses, wherein each of said data buses is operably connected between a first one of the direct memory access engines and the first shared path for communicating the first data.

20. (Currently Amended) The method of Claim 19, further including:

providing a second shared path in a second ~~clannel~~ channel interface module;

transferring second data between said first controller memory module and said second controller memory module using each of said direct memory access engines, wherein the second data passes through said second shared path;

a second plurality of said data buses, wherein each of the second plurality of said data buses is operably connected between a second one of the direct memory access engines and the second shared path for communicating the second data.

Please cancel Claim 21

22. (Previously Presented) The method of Claim 13, wherein the passive backplane includes two data busses for communicating with each of the first and second controller memory modules.